REMARKS

The Office Action mailed on October 24, 2002, has been received and reviewed.

Claims 15, 11-17, 25-28, and 33-38 are currently pending in the above-referenced application. The rejections of claims 1-5 and 25-28 have been maintained. Claims 11-17 and 33-38, which were previously allowed, now stand rejected.

Claims 11 and 33 have been amended. As the amendments to claims 11 and 33 have merely been made for the sake of clarity and not in response to the rejections that have been presented in the outstanding Office Action, they should not be read as being limited to a particular embodiment, but should be accorded the broadest scope permissible.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Tsai

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Tsai describes a method for forming shallow trench isolation structures in a semiconductor substrate. The method of Tsai includes providing a substrate 30 that includes a silicon oxide layer, which is referred to as "pad oxide layer 32," thereover and a silicon nitride layer 34 over the pad oxide layer 32. FIG. 3A. A sacrificial layer 36 of either polysilicon or silicon oxide is formed over the silicon nitride layer 34. FIG. 3B. A photomask 37 with apertures for defining trenches in the semiconductor substrate 30 is then formed over the sacrificial layer 36. FIG. 3C. Next, the trenches 38 are formed through each of layers 36, 34, and 32 and in the semiconductor substrate 30. FIG. 3D.

The photomask 37 is then removed and the silicon nitride layer 34A descumed, or etched laterally beneath the overlying sacrificial layer 36A. FIG. 3E. A thin oxide layer 39 is then formed on the surfaces of the semiconductor substrate 30 that are exposed within the trench 38A. FIG. 3F. The trench 38A is filled with a suitable dielectric material, which is referred to as "isolation material 40," such as tetraethylorthosilicate (TEOS), which also fills the descumed regions of the silicon nitride layer 34B and forms a dielectric layer over the sacrificial layer 36A. FIG. 3G. The dielectric layer and sacrificial layer 36A are then removed to expose the surface of the silicon nitride layer 34B and to form an isolation region 40A from the isolation material. FIG. 3H. Upon removal of the silicon nitride layer 34B, regions of the dielectric material that filled the descumed portion of the silicon nitride layer 34B extend laterally beyond the outer periphery of the trench 38A and over portions of the pad oxide layer 32A. FIG. 3I. Exposed portions of the pad oxide layer 32A are then removed from the surface of the semiconductor substrate 30, leaving only the isolation region 40A and portions of the pad oxide layer 32B that are shielded thereby. FIG. 3J.

By way of contrast with the method disclosed in Tsai, each of independent claims 1, 11, 25, and 33 recites a method of forming an isolation structure. In each of these methods, a layer of isolation material is applied "over [a] buffer film layer, [with] major surfaces of [the] layer of isolation material and [the] buffer film layer in contact . . ."

Each of independent claims 1, 11, 25, and 33 also recites "removing a portion of [the] isolation material above [the] buffer film layer . . ."

FIG. 3G of Tsai clearly illustrates that a major surface of the isolation material 40, when applied, contacts a major surface of the sacrificial layer 36A, which is formed from either polysilicon or silicon oxide. Col. 2, line 59, to col. 3, line 2. Thus, Tsai does not expressly or inherently describe that the major surface of the isolation material 40 contacts the major surface of the silicon nitride layer 34.

FIG. 3H of Tsai clearly shows that when a portion of the isolation material 40 is removed to form an isolation region 40A, the underlying sacrificial layer 36A is also removed.

Thus, if the sacrificial layer 36A of Tsai were considered to be the buffer film layer recited in independent claims 1, 11, 25, and 33, "a portion of [the] isolation material *above* [the]

buffer film layer" could not be removed, as recited in each of independent claims 1, 11, 25, and 33.

Moreover, if the silicon nitride layer 34B of Tsai were considered to be the buffer film layer recited in independent claims 1, 11, 25, and 33, a major surface of the isolation material 40 is not in contact with a major surface of the buffer film layer (*e.g.*, silicon nitride layer 34B), as required by each of independent claims 1, 11, 25, and 33.

Therefore, Tsai does not anticipate any of independent claims 1, 11, 25, or 33 under 35 U.S.C. § 102(e). Accordingly, under 35 U.S.C. § 102(e), each of independent claims 1, 11, 25, and 33 is allowable over Tsai.

Claims 2-4 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Each of claims 12-14 and 16 is allowable, among other reasons, as depending either directly or indirectly from claim 11, which is allowable.

Claims 26 and 27 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 25, which is allowable.

Claims 34, 35, and 37 are each allowable, among other reasons, as depending either directly or indirectly from claim 33, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1-4, 11-14, 16, 25-27, 33-35, and 37 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Tsai

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of the Examiner's Comment.

Claim 17 is allowable, among other reasons, as depending from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, as depending from claim 33, which is allowable.

Tsai in View of Lee

Claims 5, 15, 28, and 36 each stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Lee HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59 (hereinafter "Lee").

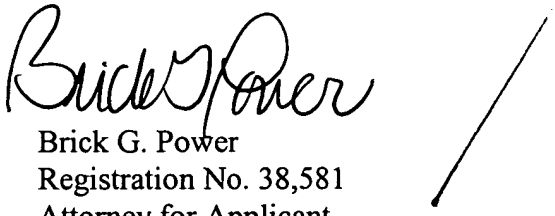
Claims 5, 15, 28, and 36 are each allowable, among other reasons, as depending from claims 1, 11, 25, and 33, respectively, each of which is allowable.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 5, 15, 17, 28, 36, and 38 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1-5, 11-17, 25-28, and 33-38 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

11. (Amended five times) A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer to expose [opposing trench edges at an intersection] <u>portions of an upper surface of said dielectric layer adjacent to an upper edge</u> of said trench [sidewalls and an upper surface of said semiconductor substrate];

applying a layer of isolation material over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material also substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

33. (Amended five times) A method of forming a capped shallow trench isolation structure for a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer to expose [opposing trench edges at an intersection] portions of an upper surface of said dielectric layer adjacent an upper edge of said trench [and an upper surface of said semiconductor substrate];

applying a layer of isolation material over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.